We claim:

1. A RRAM memory cell formed on a silicon substrate having a operative junction therein and a metal plug formed thereon, comprising:

a first oxidation resistive layer;

a first refractory metal layer;

a CMR layer;

a second refractory metal layer; and

a second oxidation resistive layer.

2. The RRAM memory cell of claim 1 wherein the oxidation resistive layers are formed of a material taken from the group of materials consisting of TiN, TaN, $TiAlN_x$, $TaAlN_x$, TaSiN, TiSiN, and RuTiN.

3. The RRAM memory cell of claim 2 wherein the oxidation resistive layers have a thickness of between about 50 nm to 300 nm.

4. The RRAM memory cell of claim 1 wherein the refractory metal layers are formed of a material taken from the group of materials consisting of Pt, Ir, IrO_2, Ru, RuO_2, Au, Ag, Rh, Pd, Ni, and Co.

5. The RRAM memory cell of claim 4 wherein the refractory metal layers have a thickness of between about 3 nm to 50 nm.

6. The RRAM memory cell of claim 1 wherein the CMR layer is formed of a material taken from the group of material consisting of CMR materials and high-temperature superconductors.

7. The RRAM memory cell of claim 6 wherein the CMR layer has a thickness of between about 50 nm to 300 nm.

8. A method of fabricating a multi-layer electrode RRAM memory cell comprising:

preparing a silicon substrate;

forming a junction in the substrate taken from the group of junctions consisting of N+ junctions and P+ junctions;

depositing a metal plug on the junction;

depositing a first oxidation resistant layer on the metal plug;

depositing a first refractory metal layer on the first oxidation resistant layer;

depositing a CMR layer on the first refractory metal layer;

depositing a second refractory metal layer on the CMR layer;

depositing a second oxidation resistant layer on the second refractory metal layer; and

completing the RRAM memory cell.

9. The method of claim 8 wherein said depositing the oxidation resistive layers includes depositing a material taken from the group of materials consisting of TiN, TaN, $TiAlN_x$, $TaAlN_x$, TaSiN, TiSiN, and RuTiN.

10. The method of claim 9 wherein said depositing the oxidation resistive layers includes depositing the oxidation resistive layers to a thickness of between about 50 nm to 300 nm.

11. The method of claim 8 wherein said depositing the refractory metal layers includes depositing a material taken from the group of materials consisting of Pt, Ir, IrO_2, Ru, RuO_2, Au, Ag, Rh, Pd, Ni, and Co.

12. The method of claim 11 wherein said depositing the refractory metal layers includes depositing the refractory metal to a thickness of between about 3 nm to 50 nm.

13. The method of claim 8 wherein said depositing a CMR layer includes depositing a layer of CMR material taken from the group of material consisting of PCMO, LPCMO and high-temperature superconductors.

14. The method of 13 wherein said depositing a CMR layer includes depositing a layer of CMR material having a thickness of between about 50 nm to 300 nm.